WHAT IS CLAIMED IS:

1. A silicon-on-insulator semiconductor device comprising:

an insulative layer formed overlying a substrate;

a source region and a drain region formed overlying the insulative layer, the source region and the drain region comprising a material having a first conductivity type;

a body region disposed between the source region and the drain region and overlying the insulative layer, the body region comprising a material having a second conductivity type;

a gate insulative layer overlying the body region;

a gate region overlying the gate insulative layer;

a diode circuit conductively coupled to the source region; and

a conductive connection coupling the gate region to the diode circuit.

2. The device of Claim 1, wherein the conductive connection comprises:

a conductive region formed overlying the gate region; and

a metal trace coupling the conductive region to the diode circuit.

3. The device of Claim 2, wherein the conductive region comprises a metallization layer.

4. The device of Claim 1, wherein the diode circuit comprises a single diode having a first region

conductively coupled to the source region, the first region having the second conductivity type, the single diode also having a second region conductively coupled to the conductive connection and having the first conductivity type.

5. The device of Claim 1, wherein the diode circuit comprises a pair of back-to-back diodes.

6. The device of Claim 5, wherein the pair of back-to-back diodes comprises a first diode coupled to the conductive connection and a second diode having a first region having the first conductivity type and a second region having the second conductivity type, the first region conductively coupled to the source region.

7. The device of Claim 6, wherein the back-to-back diodes are separated from each other by an insulative region.

8. The device of Claim 1, wherein the diode circuit comprises at least three diodes connected in series, each diode having a first region having the first conductivity type and a second region having the second conductivity type, the first region of a first one of the diodes conductively coupled to the source region and the second region of a second one of the diodes conductively coupled to the conductive connection.

9. The device of Claim 1, wherein the source region and the drain region are formed from an n-type material.

10. The device of Claim 1, wherein the source region and the drain region are formed from a p-type material.

11. The device of Claim 1, wherein the insulative layer comprises oxide.

12. A method for reducing charge damage in a silicon-on-insulator device comprising:

providing a silicon-on-insulator device having a source region and a drain region formed outwardly from an oxide layer, the oxide layer formed on a substrate and also having a gate region;

conductively coupling the source region to a diode circuit comprising at least one diode; and

conductively coupling the diode circuit to the gate region, thereby allowing charge to flow between the gate region and the source region during fabrication to prevent charge build-up, but preventing charge from flowing between the gate region and the service region during operation of the device.

13. The method of Claim 12, wherein conductively coupling the source region to a diode circuit comprises conductively coupling the source region to a diode circuit having a pair of back-to-back diodes.

14. The method of Claim 12, wherein conductively coupling the source region to a diode circuit comprises conductively coupling the source region to a diode circuit having at least three diodes connected in series.

15. The method of Claim 12, wherein the silicon-on-insulator device further comprises a metallization layer conductively coupled to the gate region, and wherein conductively coupling the diode circuit to the gate region comprises conductively coupling the gate region to the diode circuit by a metal trace.

16. The method of Claim 12, wherein the at least one diode comprises a single diode oriented with respect to the gate region and the source region such that no current may flow from the gate region to the source region during operation of the transistor.

17. A silicon-on-insulator device comprising:

a substrate;

an oxide layer formed overlying the substrate;

a source region and a drain region formed overlying the oxide layer, the source region and the drain region comprising a material having a first conductivity type;

a body region disposed between the source region and the drain region and overlying the oxide layer, the body region comprising a material having a second conductivity type;

a gate insulative layer overlying the body region;

a gate region overlying the gate insulative layer;

first and second diodes formed overlying the oxide layer and each having a first region having the first conductivity type and a second region having the second conductivity type;

wherein the first region of the first diode is conductively coupled to the source region and the second region of the first diode is conductively coupled to the second region of the second diode; and

a conductive connection coupling the gate region to the first region of the second diode.

18. The device of Claim 17, wherein the conductive connection comprises:

a conductive region formed overlying the gate region; and

a metal trace coupling the conductive region to the diode circuit.

19. The device of Claim 17, wherein the first and second diodes are separated from each other by an insulative region.

20. The device of Claim 17, wherein the source region and the drain region are formed from an n-type material.